Abstract of the Disclosure

Bit inversions occurring in memory systems and apparatus are provided. Data is acquired from a source destined for a target. As the data is acquired from the source, the set bits associated with data are tabulated. If the total number of set bits exceeds more than half of the total bits, then an inversion flag is set. When the data is transferred to the target, the bits are inverted during the transfer if the inversion flag is set.

Alternatively, an acquired data stream includes an association with an inversion bit. The inversion bit is acquired and stored separately from the data stream. As the data stream is transferred, if the inversion bit is set then the stream is inverted during the transfer of the stream to a target.

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